PLANAR CMOS-COMPATIBLE FUSION-BONDED SILICA VACUUM PACKAGES

Lin Du, Xuan Wang, and Mark G. Allen
University of Pennsylvania, Philadelphia, Pennsylvania, USA

2021 21st International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers) | 978-1-6654-1267-4/21/$31.00 ©2021 IEEE | DOI: 10.1109/TRANSDUCERS50396.2021.9495633

ABSTRACT

We present a vacuum packaging process based on standard fused silica wafer bonding combined with laser-assisted simultaneous localized fusion bonding and dicing technology. Direct bonding of fused silica wafer stacks results in an optically transparent package without introducing intermediate bonding layers. The temperature inside the package is maintained lower than 400 °C during the fabrication process to preserve CMOS compatibility. To characterize the vacuum level inside the package, white light interferometery is introduced to observe the surface topography of the package. Simulation and experimental results indicate that the vacuum level inside the package is at or below 1 Torr. Such fused silica vacuum and hermetic packages have many favorable features such as vacuum for encapsulating resonating devices, optical transparency for packaging MOEMS, biocompatibility and hermeticity for implantation applications, and transparency at radio frequencies for encapsulating electronics for wireless power and signal transmission.

KEYWORDS

Fused silica, CMOS compatible, vacuum package, localized fusion bonding, MEMS.

INTRODUCTION

Vacuum packaging technology plays an important role for microelectromechanical systems (MEMS). For MEMS devices with movable structures [1], such as resonators, gyroscopes, and accelerometers, vacuum packaging can reduce air damping, resulting in improved device performance [2, 3]. For MEMS devices with electronic components operating in harsh environments, vacuum packaging can protect the electronics from water corrosion to extend operational lifetime.

For many MEMS devices with optical components, such as imaging bolometers, scanning mirrors, and variable wavelength filters, a vacuum package with optical window is required [4]. Chu *et al*. presented a vacuum package for a 2D scanning MEMS micromirror with a glass lid as an optical window by anodic bonding with 400 °C and 500V [5]. Cheng *et al*. reported a vacuum package using localized aluminum/silicon to glass bonding with a fabricated microheater [6]. Elfrink *et al*. developed a vacuum package with glass lid by intermediate layer bonding using SU-8 [7]. Marinis *et al*. demonstrated a vacuum package with an optical window by soldering at 325 °C [4].

In our previous research, we have demonstrated a complementary metal–oxide–semiconductor (CMOS) compatible silica hermetic package by localized fusion bonding technology achieving a completely optically transparent package [8, 9]. The leakage rate of the package did not exceed 4.6×10^{-14} atm·cm^3/s. However, this package did not have an internal vacuum. To develop a vacuum package with this hermetic packaging technology would enable encapsulation of MEMS devices with movable structures; also, further reduction of the initial gas inside the package could potentially extend the lifetime of any encapsulated electronics.

In addition to the wafer bonding technology, characterization of vacuum level should be taken into consideration during design. To measure the vacuum level inside the package, usually there are two approaches: 1) to encapsulate a pressure sensor into the package, such as thermocouple gauge [10], Pirani gauge [11], microbolometer [12], or resonator whose quality factor changes with pressure [13]; or 2) to measure the surface deflection of the package (e.g. white light interferometry [14], or laser 3D profile microscopy [15]) and correlate the observed deflection with analytical results relating deflection and pressure.

In this paper, we propose to develop a fused silica vacuum and hermetic package combining traditional wafer bonding and localized fusion bonding technology. Based on our previous research and the vacuum packaging technology demonstrated in this manuscript, key features of the packages produced using this process include: 1) CMOS compatibility; 2) Optical transparency for cooperation with micro-opto-electro-mechanical systems (MOEMS); 3) Vacuum for encapsulating devices with moving structures; 4) Biocompatibility for implantation applications; and 5) Transparency at radio frequencies for encapsulating electronics for wireless power and signal transmission.

PACKAGING METHOD

Package Design

Figure 1 illustrates the packaging design, comprising: 1) a fused silica substrate wafer with a cavity; 2) a device to be encapsulated into the package; and 3) a fused silica cover wafer bonded to the substrate wafer. To demonstrate the feasibility of the packaging technology by characterization of surface deflection, we initially demonstrate a package without an encapsulated device within. In the developed package, there is a circular cover wafer of 500 μm thickness and 14 mm diameter, and a substrate wafer of the same dimension with a cavity of 4.8 μm depth and 10 mm diameter. The overall dimension of the package is 14 mm in diameter and 1 mm thick.

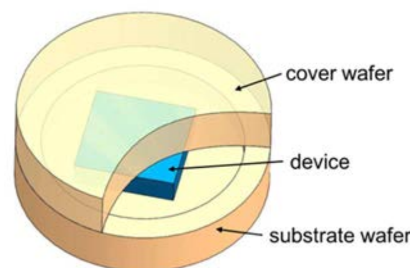

Figure 1: Schematic of package design.

Authorized licensed use limited to: Lawrence Berkeley National Laboratory. Downloaded on November 09,2023 at 22:07:33 UTC from IEEE Xplore. Restrictions apply.

Mechanical Simulation

To determine the relationship between the vacuum level inside the package and the resultant package surface deflection, as well as to identify the appropriate dimensions that could provide a reasonable response for characterization, a COMSOL Multiphysics simulation is performed.

In this simulation for deflection of the cover wafer, there is a circular wafer of 500 µm thickness and 14 mm diameter. The region where the cover wafer is bonded to the substrate wafer is fixed. The pressure inside the package is defined as the package pressure, and the pressure external to the package is defined as the external pressure. For the purposes of this work, the external pressure will be taken to be atmospheric.

When the package pressure is held at 1 Torr, the resultant deflection of the cover wafer is shown in Figure 2(a). The red color indicates the minimum deflection and the blue color indicates the maximum deflection, bending toward the substrate wafer. The deflection of the cover wafer at various package pressures of 1 Torr, 20 Torr, 100 Torr, 200 Torr, and 300 Torr is presented in Figure 2(b). As expected, when the package pressure is 1 Torr, the pressure difference across the package is the largest (759 Torr); hence, the package surface has the maximum deflection.

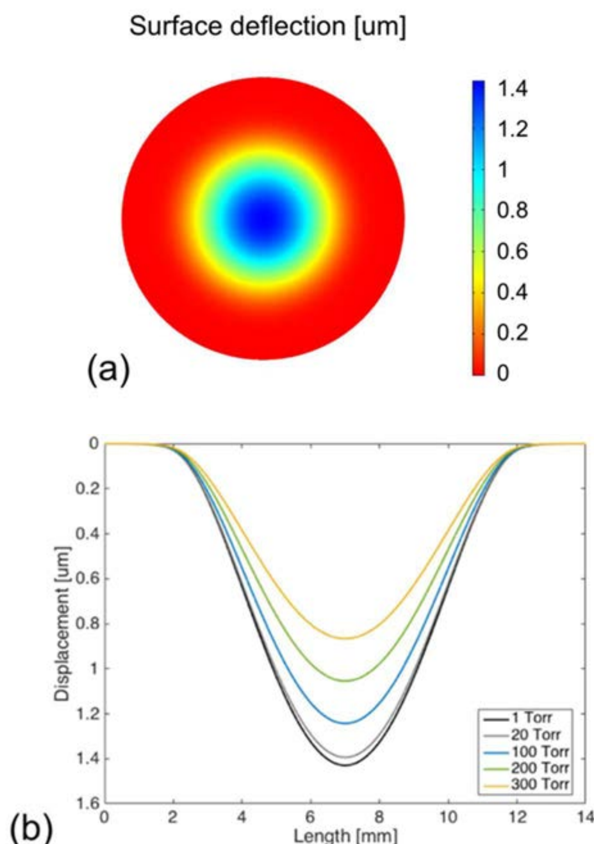

Figure 2: Simulation of cover wafer: (a) surface deflection for a package pressure of 1 Torr; (b) surface deflection when the package pressure is parametrically varied to 1 Torr, 20 Torr, 100 Torr, 200 Torr, and 300 Torr. For both simulations, the pressure outside the package is taken to be atmospheric (760 Torr).

FABRICATION PROCESS

The fabrication process is based on the combination of a temperature-limited, modified wafer prebonding procedure in a vacuum environment, followed by CO_2 laser-assisted localized fusion bonding and dicing technology. The process is comprised of four steps: (1) fabrication of the substrate wafer with a cavity; (2) cleaning of the cover wafer and the substrate wafer; (3) direct bonding of cover wafer and substrate wafer in a vacuum environment using wafer bonder; and (4) CO_2 laser-assisted localized fusion bonding and dicing of the wafer stacks to create both the final seal and to singulate the packages.

Fabrication begins with cleaning a 4-inch fused silica wafer of 500 um thickness using acetone, methanol, and isopropanol (IPA). Positive photoresist SPR220-7.0 is spin coated on the wafer with a speed of 500 rpm for 10 seconds and 3000 rpm for 50 seconds. Subsequently, the wafer is placed on a hot plate at 110 °C for 3 minutes for soft bake (Figure 3(a)). Lithography process is performed to expose a circular region of 10 mm in diameter. The wafer with photoresist on top is then developed in MF-26A to define the pattern for a subsequent etching process, as shown in Figure 3(b). Afterwards, reactive ion etching (RIE) is implemented to achieve a cylindrical cavity of 4.8 µm depth on the substrate wafer (Figure 3(c)). Subsequently, the photoresist is stripped with acetone.

Cleaning of the cover wafer (4-inch, 500 um thick) and the fabricated substrate wafer with cavity are accomplished with piranha solution. The wafers are immersed in piranha solution ($H_2SO_4 : H_2O=3:1$) at 85 °C for 20 minutes, rinsed with deionized (DI) water, and dried with spin rinse dryer. Immediately after the cleaning process, the two wafers are manually aligned and bonded by Van der Waals force at room temperature by placing the cover wafer facing the cavity of the substrate wafer to avoid contamination during transfer (Figure 3(d)).

To perform a direct bonding of cover wafer and substrate wafer in vacuum environment, the two wafers are installed in a wafer bonder (EVG510) with a spacer in between the cover wafer and substrate wafer (Figure 3(e)). The chamber is then evacuated to 1 mbar and the spacer is removed from the wafer stack. A metal disc is then placed in contact with the cover wafer to apply a force of 5000 N at 400 °C for 17 hours, as presented in Figure 3(f). Once prebonding is completed, a CO_2 laser assisted localized fusion bonding and dicing of the fused silica wafer stack is performed to achieve a hermetic sealing (Figure 3(g)).

Authorized licensed use limited to: Lawrence Berkeley National Laboratory. Downloaded on November 09,2023 at 22:07:33 UTC from IEEE Xplore. Restrictions apply.

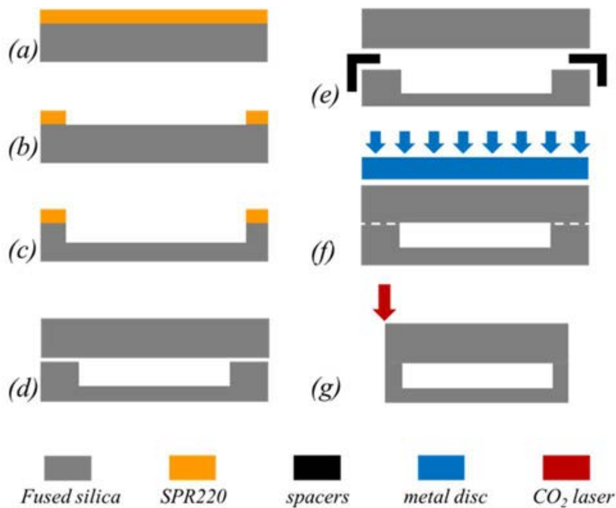

Figure 3: Fabrication process of a vacuum package: (a) clean substrate wafer, spin coat photoresist, and soft bake; (b) exposure, photoresist development; (c) RIE to form a cavity on substrate wafer; (d) clean cover wafer and substrate wafer, rinse, and dry; (e) install the wafer stacks in wafer bonder; (f) direct bonding in vacuum environment; (g) localized fusion bonding.

Figure 4 shows the fabricated fused silica vacuum package. The entire package is 14 mm in diameter and the circular shape inside is 10 mm in diameter which corresponds to the cylindrical cavity region. At the cavity region, Newton rings are observed indicating the proximity of the vacuum-induced deflection of the upper package toward the lower package substrate (Figure 4(a)). From the side view, the two 500 µm thick wafers are bonded and the total thickness is 1 mm, as presented in Figure 4(b). A tilted view of the package is presented in Figure 4(c). As an advantage of laser-assisted technology, packages with arbitrary shapes could be achieved (Figure 4(d)).

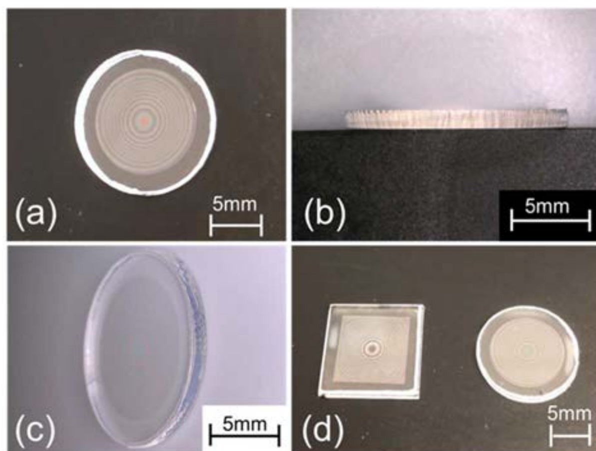

Figure 4: Package prototypes (a) top view: 14 mm diameter package with Newton rings at the 10 mm diameter cylindrical cavity region; (b) side view: two 500 µm thick wafers are bonded and the total thickness is 1 mm; (c) tilted view; (d) package of square and circular shapes.

VACUUM CHARACTERIZATION

In order to investigate the vacuum level inside the package, white light interferometery (Zygo NewView 7300) is exploited to characterize the topography of the package. Correlating the observation with simulation results allows determination of the encapsulated vacuum level.

A surface topography image of the package after the direct bonding using wafer bonder (but prior to the laser-assisted fusion bonding process) is shown in Figure 5(a). The red color indicates a higher topography and the blue color indicates a lower topography. Therefore, Figure 5(a) presented a package surface that is higher at the periphery region and lower near the center, indicating the surface is concave, as expected.

Figure 5(b) shows the topographical image after the laser-assisted fusion bonding process. Figure 5(b) again indicates a package surface that is higher at the periphery region and lower in the center, indicating the concave surface has been maintained. The circular shape of the package is defined through the laser-assisted bonding process, resulting in a cylindrical package with smooth contour. There are some black scratches at the peripheral region of the package, probably due to the re-deposition of fused silica material attached to the surface during the bonding procedure.

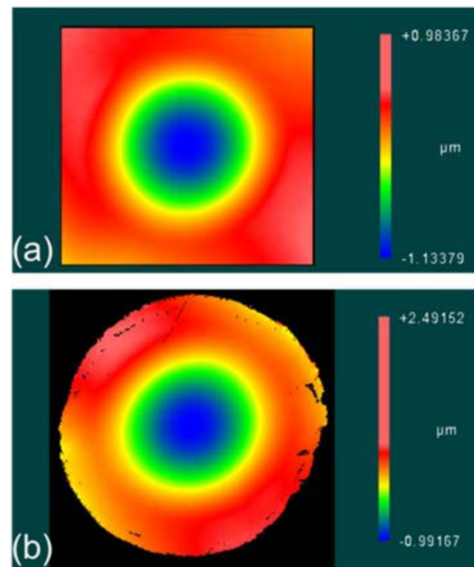

Figure 5: Topography of package surface: (a) before fusion bonding; (b) after fusion bonding.

To investigate the vacuum level inside the package, the experimental results of Figure 5 are compared with the simulation results of Figure 2. As shown in Figure 6, prior to the fusion bonding process, the experimental deflection is comparable with the simulation when the package pressure is 1 Torr. After the fusion bonding, the experimental deflection is comparable with the simulation when the package pressure is 20 Torr. Three possible sources of the change of surface topography measured are: 1) The measurement result is performed along a randomly selected profile on the package surface. Therefore, the measurement before and after the bonding process is not the same profile; 2) The package is distorted slightly during the bonding process, as shown in Figure 6(b) that the symmetry of the surface topography is disturbed that the measurement after bonding is not accurately indicating the vacuum inside package; 3) Water vapor may be desorbed

Authorized licensed use limited to: Lawrence Berkeley National Laboratory. Downloaded on November 09,2023 at 22:07:33 UTC from IEEE Xplore. Restrictions apply.

from the surface and/or generated during the fusion bonding process and escape into the cavity [16]. Further encapsulation of a resonating device for characterization could improve the measurement resolution. Nonetheless, this experiment demonstrates the feasibility of maintaining the vacuum status of the package during the fusion bonding portion of the packaging fabrication process.

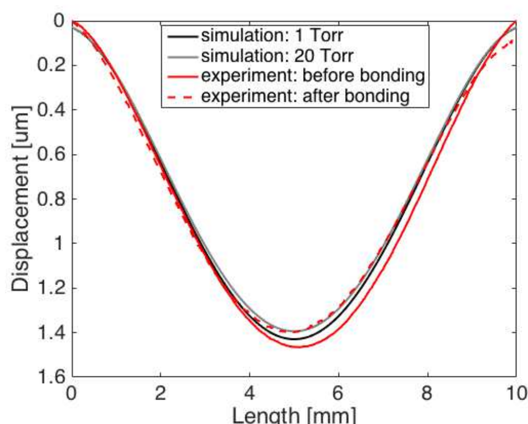

Figure 6: Comparison between simulation and experimental vacuum level inside the package.

CONCLUSIONS

We achieve a planar, vacuum-encapsulating silica package by exploiting traditional wafer bonding and laser-assisted localized fusion bonding and dicing technology. The package is completely transparent and CMOS compatible. COMSOL simulation is performed to investigate the surface deflection of package when there is vacuum inside package. To determine the vacuum level inside the package, white light interferometery is implemented to measure the topography of the package. Comparing the experimental results with simulation, the vacuum level inside the package reaches 1 Torr.

REFERENCES

[1] C. S. Premachandran, S. C. Chong, S. Liw, and R. Nagarajan. "Design, fabrication and testing of wafer level vacuum package for MEMS device," in *56th Electronic Components and Technology Conference 2006*, San Diego, CA, 2006.
[2] M. Esashi, "Wafer level packaging of MEMS, " *Journal of Micromechanics and Microengineering*, vol. 18, no. 7, p. 073001, 2008.
[3] L. Lin, "MEMS post-packaging by localized heating and bonding, " *IEEE Transactions on Advanced Packaging*, vol. 23, no. 4, pp. 608–616, 2000.
[4] T. F. Marinis, J. W. Soucy, and J. G. Lawrence. "Vacuum sealed MEMS package with an optical window," in *2008 58th Electronic Components and Technology Conference*, Lake Buena Vista, FL, 2008.
[5] H. M. Chu, T. Sasaki, and K. Hane. "Design, fabrication, and vacuum package process for high performance of 2D scanning MEMS micromirror," in *2011 16th International Solid-State Sensors, Actuators and Microsystems Conference*, Beijing, 2011.
[6] Y. T. Cheng *et al.*, "Vacuum packaging technology using localized aluminum/silicon-to-glass bonding," *Journal of Microelectromechanical Systems*, vol. 11, no. 5, pp. 556-565, Oct. 2002.
[7] R. Elfrink *et al.*, "Vacuum packaged MEMS piezoelectric vibration energy harvesters," in *Proc. PowerMEMS*, Washington DC, 2009.
[8] L. Du and M. G. Allen, "Silica hermetic packages based on laser patterning and localized fusion bonding," in *2018 IEEE Micro Electro Mechanical Systems*, Belfast, UK, 2018.
[9] L. Du and M. G. Allen, "CMOS compatible hermetic packages based on localized fusion bonding of fused silica," *Journal of Microelectromechanical Systems*, vol. 28, no. 4, pp. 656-665, 2019.
[10] G. Wu, D. Xu, X. Sun, B. Xiong, Y. Wang, "Wafer-level vacuum packaging for microsystems using glass frit bonding." in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 10 pp. 1640-1646, 2013.
[11] S. H. Lee, J. Mitchell, W. Welch, S. Lee, K. Najafi, "Wafer-level vacuum/hermetic packaging technologies for MEMS," *Reliability, Packaging, Testing, and Characterization of Mems/Moems and Nanodevices IX*, San Francisco, CA, 2010.
[12] R. Gooch, T. Schimert, W. McCardel, and B. Ritchey, "Wafer-level vacuum packaging for MEMS." *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 17, no. 4, pp. 2295-2299, 1999.
[13] Dienel, Marco, *et al*. "On the influence of vacuum on the design and characterization of MEMS," *Vacuum*, vol. 86, no. 5, pp. 536-546, 2012.
[14] X. Wang, S. J. Bleiker, M. Antelius, G. Stemme, F. Niklaus, "Wafer-level vacuum packaging enabled by plastic deformation and low-temperature welding of copper sealing rings with a small footprint," *Journal of microelectromechanical systems,* vol. 26, no. 2, pp. 357-365, 2017.
[15] K. Ikushima, A. Baba, M. Kyougoku, K. Sawada, M. Ishida, "Fabrication and characterization of a pixel level micro vacuum package for infrared imager." in *17th IEEE International Conference on Micro Electro Mechanical Systems. Maastricht MEMS 2004 Technical Digest*., Maastricht, Netherlands, 2004.
[16] H. Moriceau *et al*., "Overview of recent direct wafer bonding advances and applications," *Adv. Nat. Sci.: Nanosci. Nanotechnol*., vol. 1, pp. 043004, 2010.

ACKNOWLEDGEMENT

This work was carried out in part at the Singh Center for Nanotechnology, which is supported by the NSF National Nanotechnology Coordinated Infrastructure Program under grant NNCI-2025608.

CONTACT

*L. Du, tel: +1-267-693-7813; dulin@seas.upenn.edu

Authorized licensed use limited to: Lawrence Berkeley National Laboratory. Downloaded on November 09,2023 at 22:07:33 UTC from IEEE Xplore. Restrictions apply.